COREXOM R6490Q SOM

COREXOM R5430Q SOM

DATASHEET

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2025/11/06

Revision History

Rev.	Date	Description
0.1	2024/04/23	Draft
0.2	2024/11/06	Added new section 2.3.16 for GPIO pins collection Updated section 2.3.1 with pins V2 and V3, and NC pins Added new section 2.3.21 Miscellaneous for un-group signals
0.3	2024/11/20	Updated section 2.3.7 to open PCIe0 related pins function on LGA pad
0.4	2025/05/15	Modified Model name from R6490C to R6490Q to apply rule Add new version R5430Q related data Add contents of section 4.3 Thermal Characteristics Add new section 4.4 Packaging information Updated section 6 Product Marking information contents
0.5	2025/06/20	Add new section 6. Compliance Statement
0.6	2025/07/12	Correction SM_GPIO_63 SE# typo in 2.3.26 GPIO Correction the URL in section 4.3 Thermal Characteristics
	2025/08/28	Add new section 4.5 Temperature and Humidity
0.7	2025/11/06	Add carton label information in section 4.4 Adjust the P/N list as neutral way in section 6 Product Marking, to become not be bundled with SOM revision.

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About This Document

- Illustrations in this documentation might look different from your product.
- Depending on the model, some optional accessories, features, and software programs might not be available on your device.
- Depending on the version of operating systems and programs, some user interface instructions might not be applicable to your device.
- Documentation content is subject to change without notice. Coretronic Reality Inc. (CRI) makes constant improvements on the documentation of your computer, including this guidebook.

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1. Introduction

CRI COREXOM R6490Q/R5430Q SOM (System on Module) is a high-performance intelligent module, integrating Android, based on Qualcomm® Snapdragon™ QCS6490 /QCS5430 SoC. It integrates the advanced 6 nm processor with superior performance and power efficiency, as well as high AI capability (up to 12.5 TOPS). It is featured with 5 x 4-lane MIPI CSI D-PHY (2 of them compatible to support 3-lane MIPI CSI C-PHY which is up to 48M camera). It also has a rich set of peripheral interfaces, including both USB 3.1 and USB 2.0 concurrency and PCIe.

The R6490Q/R5430Q SOM is a high performance AIoT SOM for building Handheld Devices, Industrial Robots, Service Robots, Drones and Digital Signage, providing customers with hardware interfaces and software SDK to validate functions and build the prototype quickly, and also provide for mass production.

1.1 Features

The following table shows the detailed features of QCS6490/QCS5430 and R6490Q /R5430Q SOM

Key features of QCS6490/QCS5430 SoC

Item	Description
CPU	Qualcomm® Kryo™ CPU 670 built on Arm v8 Cortex technology QCS6490 : ● Kryo Prime : one high-performance core up to 2.7 GHz ● Kryo Gold : three high-performance cores at 2.4 GHz ● Kryo Silver : four low-power cores at 1.9 GHz QCS5430 FP1 : (through FW license can upgrade to FP2, FP2.5, FP3) ● Kryo Gold : two high-performance cores at 2.1 GHz ● Kryo Silver : four low-power cores at 1.8 GHz
GPU	QCS6490 : ● Adreno GPU 643@812MHz (MH3.0 95+fps) QCS5430 FP1 : ● Adreno GPU 642L@315MHz (MH3.0 45-48fps) ● OpenGL ES 3.2, Vulkan 1.x ● OpenCL 2.0, DX FL12
DSP and AI	6th Gen Qualcomm AI Engine QCS6490 : ● 2x HVX 4K-HMX 1.45GHZ (12.15 INT8 TOPS) QCS5430 FP1 :

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Item	Description
	● 2x HVX 2K-HMX 912MHZ (~3.5 INT8 TOPS) Compute Hexagon DSP with dual HVX and Hexagon Co-processor (Hexagon CP) 2.0 and Hexagon Tensor Accelerator ● Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, and so on ● The Hexagon CP is a vision and imaging hardware accelerator to offload and accelerate
Display	Adreno DPU 1075 : QCS6490 : ● Maximum resolution for internal panel : FHD+(2520x1080) @144 Hz QCLTM, HDR10+, WCG, improved QCS5430 : ● Maximum resolution for internal panel : FHD+(2520x1080) @120 Hz QCLTM, HDR10+, WCG, improved ● inline rot, rounded corner, SPR, De-Mura, CWB-ROI ● One 4-lane; DSI D-PHY 1.2 or C-PHY 1.2; VESA DSC 1.2 ● 4K@60FPS display support over DisplayPort (USB3 + DisplayPort concurrency)
Adreno VPU (Video Processing Unit)	Adreno VPU 633 – fifth-generation UHD video processing unit ● Video Encode : Up to 4K@30fps for H.264/H.265 ● Video Decode : Up to 4K@60fps for H.264/H.265/VP9 ● Video concurrency: 1080P@60FPS decode and 1080P@60FPS encode/4K@30FPS decode + 1080P@30FPS encode ● HDR playback: Support for HDR10 and HDR10+ ● HFR capture: 720P@480FPS or 1080P@240FPS
Camera support	QCS6490 : ● Qualcomm Spectra 570L: 36 + 22MP@30FPS / 3x 22MP@30FPS ● Qualcomm Spectra 570L ISP supports connectivity to multiple cameras due to five C-PHY/D-PHY interfaces. ● Real-time sensor input resolution: 22 + 22 + 22 MP ● Three IFE + two IFE lite, up to eight sensors, five concurrent MIPI CSI configurable in 4 + 4 +4 + 4 + 4 configurations ● 5x D-PHY v1.2 /C-PHY v1.2 QCS5430 FP1 : ● Qualcomm Spectra 570L: 22 + 22MP@30FPS ● Qualcomm Spectra 570L ISP supports connectivity to multiple cameras due to four C-PHY/D-PHY interfaces. ● Real-time sensor input resolution: 22 + 22 MP

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Item	Description
	● Two IFE + two IFE lite, up to eight sensors, four concurrent MIPI CSI ● 4x D-PHY v1.2 /C-PHY v1.2

Key features of R6490Q/R5430Q SOM

R6490Q and R5430Q are pin to pin compatible by LGA package.

Item	Description
Processor	R6490Q : Snapdragon™ QCS6490 R5430Q : Snapdragon™ QCS5430 FP1
Memory	LPDDR4X 8GB + UFS2.x 128GB for R6490Q LPDDR4X 4GB + UFS2.x 64GB for R5430Q
Display I/F	1 x MIPI-DSI 4-lane, 4K@60fps display support over DisplayPort
Camera I/F	R6490Q : 5x 4 data lane MIPI CSI D-PHY R5430Q : 4x 4 data lane MIPI CSI D-PHY (2 of them compatible with 3-trio lane MIPI CSI C-PHY up to 48M)
Audio I/F	● 2x SoundWire interface ● 3x DMIC interface
USB	1x USB 3.1 with DisplayPort 1x USB 2.0
PCIe	1x 2-lane PCIe Gen3.0 (PCIe1), 1x 1-lane PCIe Gen3.0 (PCIe0)
Peripheral (QUP) I/F	● 1x SDC for SD card ● QUPs (UART/I2C/SPI) ● GPIOs
Package	LGA
Dimensions	42.5mm x 43.0mm x 2.95mm
Operation System	Android, Ubuntu, Windows IoT, Qualcomm-Linux

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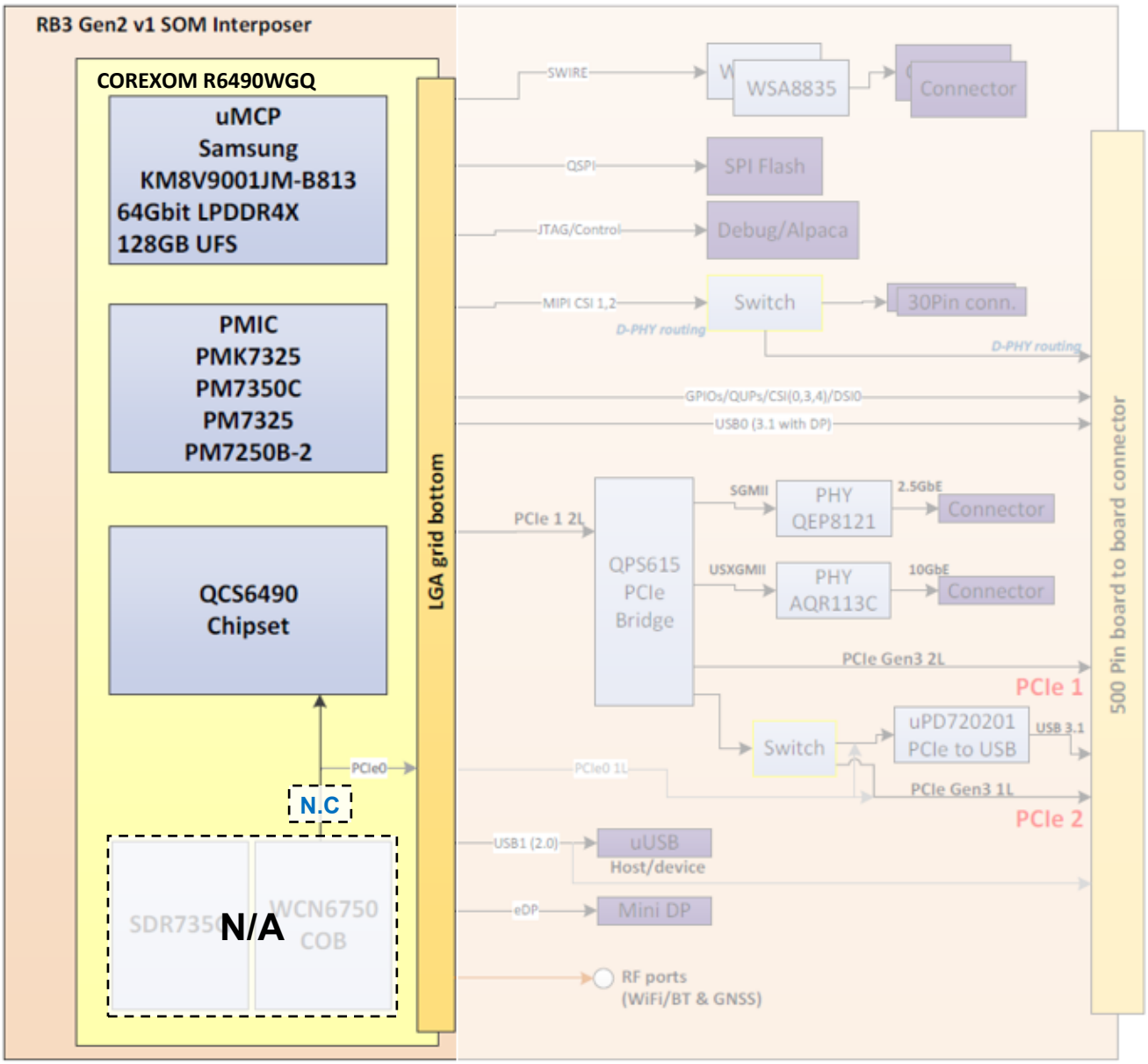
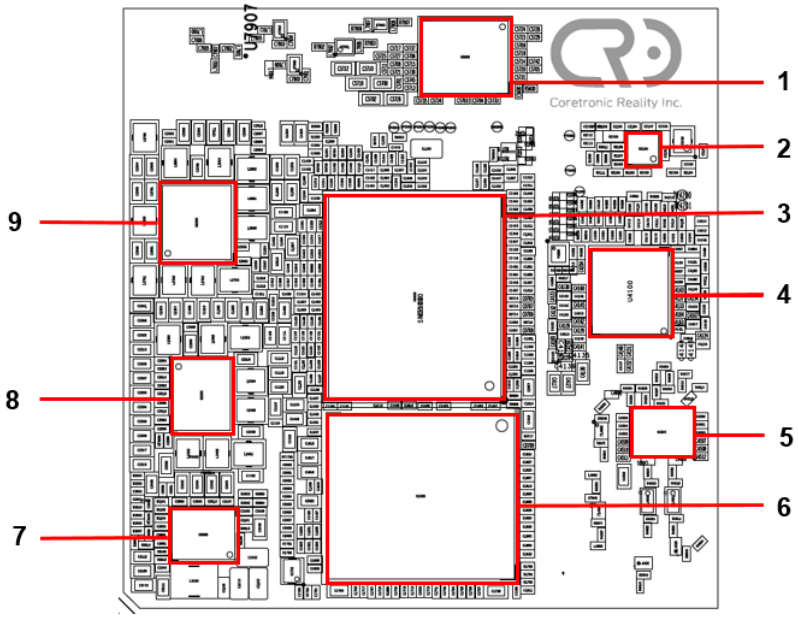
1.2 Block Diagram

R6490Q/R5430Q SOM and application interposer Hardware Block diagram is shown in below as reference



1.3 Major components location

Below picture identify the major components and connectors found on the top of the COREXOM R6490Q/R5430Q



1	(N.A)	6	uMCP LPDDR4 8GB + UFS 128GB
2	PMK7325 PMIC		
3	QCS6490/QCS5430 SoC	7	PM7250B PMIC
4	(N.A)	8	PM7325 PMIC
5	(N.A)	9	PM7350C PMIC

1.4 SMT assembly guide and Stencil design

Please refer document “COREXOM R6490WGQ SOM DFM SMT Assembly Guide” in detail.

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2. Interface Specification

This chapter introduces all the interfaces definition, purpose to guide developer easy to design and verification on CRI COREXOM R6490Q/R5430Q SOM.

2.1 Interface pin type definition

Type	Description
AI	Analog input
AO	Analog output
B, BIO	Bidirectional digital CMOS I/O
CSI	MIPI CSI related circuits and I/O
DSI	MIPI DSI related circuits and I/O
DI	Digital CMOS input
DO	Digital CMOS output
H	High voltage tolerance
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters, and options following the colon (:) NP: pdpukp = default no-pull PD: nppukp = default pull-down PU: nppdkp = default pull-up KP: nppdpu = default keeper
KP	Contains an internal weak keeper device (cannot drive external buses)
NP	Contains no internal pull
OD	Open drain
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PX3	Power for PX3 group by 1.8V
PX2	Power for SDC PX2 group by 2.95V (option 1.8V)
USB	USB SS/HS/FS related circuits and I/O
PCIe	PCIe related circuits and I/O

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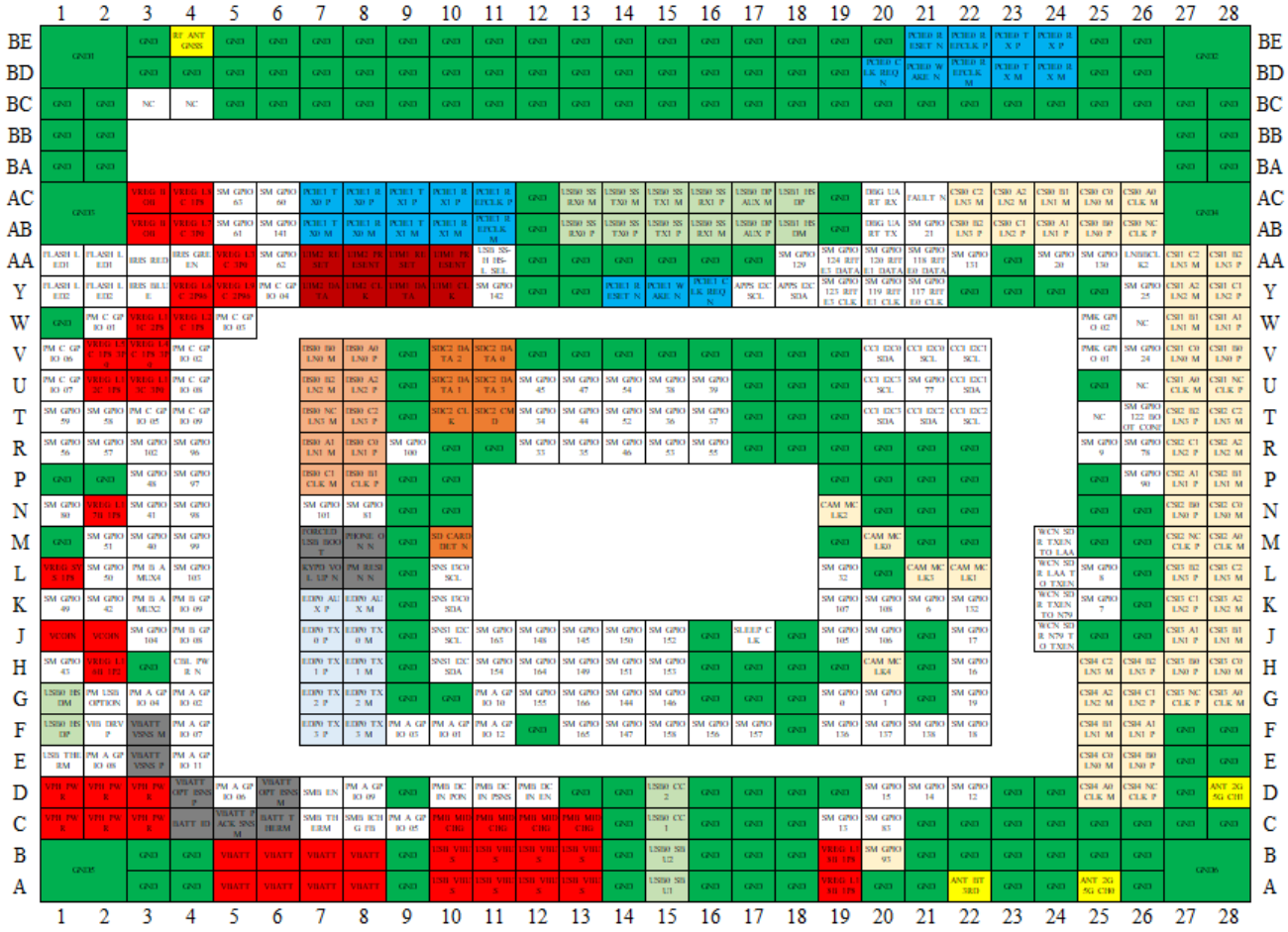
2.2 SOM Interface LGA pins Map



Power	RF ANT	DSI
GND	USB & CC & SBU	eDP
PON & Battery I/F	PCIE & Control	SDC
	CSI & CCI & MCLK	UIM

SOM Top View see through

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14
BE	GND1		GND	RF_ANT_GNSS	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
BD			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
BC	GND	GND	NC	NC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
BB	GND	GND												
BA	GND	GND												
AC	GND3		VREG_BOB	VREG_L8C_1P8	SM_GPIO_63	SM_GPIO_60	PCIE1_TX0_P	PCIE1_RX0_P	PCIE1_TX1_P	PCIE1_RX1_P	PCIE1_REFCLK_P	GND	USB0_SS_RX0_M	USB0_SS_TX0_M
AB			VREG_BOB	VREG_L7C_3P0	SM_GPIO_61	SM_GPIO_141	PCIE1_TX0_M	PCIE1_RX0_M	PCIE1_TX1_M	PCIE1_RX1_M	PCIE1_REFCLK_M	GND	USB0_SS_RX0_P	USB0_SS_TX0_P
AA	FLASH_LED1	FLASH_LED1	IRIS_RED	IRIS_GREEN	VREG_L3C_3P0	SM_GPIO_62	UIM2_RESET	UIM2_PRESENT	UIM1_RESET	UIM1_PRESENT	USB_SS-H_HS-L_SEL	GND	GND	GND
Y	FLASH_LED2	FLASH_LED2	IRIS_BLUE	VREG_L6C_2P96	VREG_L9C_2P96	PM_C_GPIO_04	UIM2_DATA	UIM2_CLK	UIM1_DATA	UIM1_CLK	SM_GPIO_142	GND	GND	PCIE1_RESET_N
W	GND	PM_C_GPIO_01	VREG_L11C_2P8	VREG_L2C_1P8	PM_C_GPIO_03									
V	PM_C_GPIO_06	VREG_L5C_1P8_3P0	VREG_L4C_1P8_3P0	PM_C_GPIO_02			DSI0_B0_LN0_M	DSI0_A0_LN0_P	GND	SDC2_DATA_2	SDC2_DATA_0	GND	GND	GND
U	PM_C_GPIO_07	VREG_L12C_1P8	VREG_L13C_3P0	PM_C_GPIO_08			DSI0_B2_LN2_M	DSI0_A2_LN2_P	GND	SDC2_DATA_1	SDC2_DATA_3	SM_GPIO_45	SM_GPIO_47	SM_GPIO_54
T	SM_GPIO_59	SM_GPIO_58	PM_C_GPIO_05	PM_C_GPIO_09			DSI0_NC_LN3_M	DSI0_C2_LN3_P	GND	SDC2_CLK	SDC2_CMD	SM_GPIO_34	SM_GPIO_44	SM_GPIO_52
R	SM_GPIO_56	SM_GPIO_57	SM_GPIO_102	SM_GPIO_96			DSI0_A1_LN1_M	DSI0_C0_LN1_P	SM_GPIO_100	GND	GND	SM_GPIO_33	SM_GPIO_35	SM_GPIO_46
P	GND	GND	SM_GPIO_48	SM_GPIO_97			DSI0_C1_CLK_M	DSI0_B1_CLK_P	GND	GND				
N	SM_GPIO_80	VREG_L17B_1P8	SM_GPIO_41	SM_GPIO_98			SM_GPIO_101	SM_GPIO_81	GND	GND				
M	GND	SM_GPIO_51	SM_GPIO_40	SM_GPIO_99			FORCED_USB_BOOT	PHONE_ON_N	GND	SD_CARD_DET_N				
L	VREG_SYS_1P8	SM_GPIO_50	PM_B_AMUX4	SM_GPIO_103			KYPD_VOL_UP_N	PM_RESIN_N	GND	SNS_I3C0_SCL				
K	SM_GPIO_49	SM_GPIO_42	PM_B_AMUX2	PM_B_GPIO_09			EDP0_AUX_P	EDP0_AUX_M	GND	SNS_I3C0_SDA				
J	VCOIN	VCOIN	SM_GPIO_104	PM_B_GPIO_08			EDP0_TX0_P	EDP0_TX0_M	GND	SNS1_I2C_SCL	SM_GPIO_163	SM_GPIO_148	SM_GPIO_145	SM_GPIO_150
H	SM_GPIO_43	VREG_L16B_1P2	GND	CBL_PWR_N			EDP0_TX1_P	EDP0_TX1_M	GND	SNS1_I2C_SDA	SM_GPIO_154	SM_GPIO_164	SM_GPIO_149	SM_GPIO_151
G	USB0_HS_DM	PM_USB_OPTION	PM_A_GPIO_04	PM_A_GPIO_02			EDP0_TX2_P	EDP0_TX2_M	GND	GND	PM_A_GPIO_10	SM_GPIO_155	SM_GPIO_166	SM_GPIO_144
F	USB0_HS_DP	VIB_DRV_P	VBATT_VSNS_M	PM_A_GPIO_07			EDP0_TX3_P	EDP0_TX3_M	PM_A_GPIO_03	PM_A_GPIO_01	PM_A_GPIO_12	GND	SM_GPIO_165	SM_GPIO_147
E	USB_THERM	PM_A_GPIO_08	VBATT_VSNS_P	PM_A_GPIO_11										
D	VPH_PWR	VPH_PWR	VPH_PWR	VBATT_OPT_ISNS_P	PM_A_GPIO_06	VBATT_OPT_ISNS_M	SMB_EN	PM_A_GPIO_09	GND	PMB_DC_IN_PON	PMB_DC_IN_PSNS	PMB_DC_IN_EN	GND	GND
C	VPH_PWR	VPH_PWR	VPH_PWR	BATT_ID	VBATT_PACK_SNS_M	BATT_THERM	SMB_THERM	SMB_ICHG_FB	PM_A_GPIO_05	PMB_MID_CHG	PMB_MID_CHG	PMB_MID_CHG	PMB_MID_CHG	GND
B	GND5		GND	GND	VBATT	VBATT	VBATT	VBATT	GND	USB_VBUS	USB_VBUS	USB_VBUS	USB_VBUS	GND
A			GND	GND	VBATT	VBATT	VBATT	VBATT	GND	USB_VBUS	USB_VBUS	USB_VBUS	USB_VBUS	GND
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

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15	16	17	18	19	20	21	22	23	24	25	26	27	28	
GND	GND	GND	GND	GND	GND	PCIE0_RESET_N	PCIE0_REFCLK_P	PCIE0_TX_P	PCIE0_RX_P	GND	GND	GND2		BE
GND	GND	GND	GND	GND	PCIE0_CLK_REQ_N	PCIE0_WAKE_N	PCIE0_REFCLK_M	PCIE0_TX_M	PCIE0_RX_M	GND	GND			BD
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	BC
												GND	GND	BB
												GND	GND	BA
USB0_SS_TX1_M	USB0_SS_RX1_P	USB0_DP_AUX_M	USB1_HS_DP	GND	DBG_UART_RX	FAULT_N	CSI0_C2_LN3_M	CSI0_A2_LN2_M	CSI0_B1_LN1_M	CSI0_C0_LN0_M	CSI0_A0_CLK_M	GND4		AC
USB0_SS_TX1_P	USB0_SS_RX1_M	USB0_DP_AUX_P	USB1_HS_DM	GND	DBG_UART_TX	SM_GPIO_21	CSI0_B2_LN3_P	CSI0_C1_LN2_P	CSI0_A1_LN1_P	CSI0_B0_LN0_P	CSI0_NC_CLK_P			AB
GND	GND	GND	SM_GPIO_129	SM_GPIO_124_RFFE3_DATA	SM_GPIO_120_RFFE1_DATA	SM_GPIO_118_RFFE0_DATA	SM_GPIO_131	GND	SM_GPIO_20	SM_GPIO_130	LNBBCLK2	CSI1_C2_LN3_M	CSI1_B2_LN3_P	AA
PCIE1_WAKE_N	PCIE1_CLK_REQ_N	APPS_I2C_SCL	APPS_I2C_SDA	SM_GPIO_123_RFFE3_CLK	SM_GPIO_119_RFFE1_CLK	SM_GPIO_117_RFFE0_CLK	GND	GND	GND	GND	SM_GPIO_25	CSI1_A2_LN2_M	CSI1_C1_LN2_P	Y
										PMK_GPIO_02	NC	CSI1_B1_LN1_M	CSI1_A1_LN1_P	W
GND	GND	GND	GND	GND	CCI_I2C0_SDA	CCI_I2C0_SCL	CCI_I2C1_SCL			PMK_GPIO_01	SM_GPIO_24	CSI1_C0_LN0_M	CSI1_B0_LN0_P	V
SM_GPIO_38	SM_GPIO_39	GND	GND	GND	CCI_I2C3_SCL	SM_GPIO_77	CCI_I2C1_SDA			GND	NC	CSI1_A0_CLK_M	CSI1_NC_CLK_P	U
SM_GPIO_36	SM_GPIO_37	GND	GND	GND	CCI_I2C3_SDA	CCI_I2C2_SDA	CCI_I2C2_SCL			NC	SM_GPIO_122_BOOT_CONFIG_	CSI2_B2_LN3_P	CSI2_C2_LN3_M	T
SM_GPIO_53	SM_GPIO_55	GND	GND	GND	GND	GND	GND			SM_GPIO_9	SM_GPIO_78	CSI2_C1_LN2_P	CSI2_A2_LN2_M	R
				GND	GND	GND	GND			GND	SM_GPIO_90	CSI2_A1_LN1_P	CSI2_B1_LN1_M	P
				CAM_MCLK2	GND	GND	GND			GND	GND	CSI2_B0_LN0_P	CSI2_C0_LN0_M	N
				GND	CAM_MCLK0	GND	GND		WCN_SDR_TXEN_TO_LAA	GND	GND	CSI2_NC_CLK_P	CSI2_A0_CLK_M	M
				SM_GPIO_32	GND	CAM_MCLK3	CAM_MCLK1		WCN_SDR_LAA_TO_TXEN	SM_GPIO_8	GND	CSI3_B2_LN3_P	CSI3_C2_LN3_M	L
				SM_GPIO_107	SM_GPIO_108	SM_GPIO_6	SM_GPIO_132		WCN_SDR_TXEN_TO_N79	SM_GPIO_7	GND	CSI3_C1_LN2_P	CSI3_A2_LN2_M	K
SM_GPIO_152	GND	SLEEP_CLK	GND	SM_GPIO_105	SM_GPIO_106	GND	SM_GPIO_17		WCN_SDR_N79_TO_TXEN	GND	GND	CSI3_A1_LN1_P	CSI3_B1_LN1_M	J
SM_GPIO_153	GND	GND	GND	GND	CAM_MCLK4	GND	SM_GPIO_16			CSI4_C2_LN3_M	CSI4_B2_LN3_P	CSI3_B0_LN0_P	CSI3_C0_LN0_M	H
SM_GPIO_146	GND	GND	GND	SM_GPIO_0	SM_GPIO_1	GND	SM_GPIO_19			CSI4_A2_LN2_M	CSI4_C1_LN2_P	CSI3_NC_CLK_P	CSI3_A0_CLK_M	G
SM_GPIO_158	SM_GPIO_156	SM_GPIO_157	GND	SM_GPIO_136	SM_GPIO_137	SM_GPIO_138	SM_GPIO_18			CSI4_B1_LN1_M	CSI4_A1_LN1_P	GND	GND	F
										CSI4_C0_LN0_M	CSI4_B0_LN0_P	GND	GND	E
USB0_CC2	GND	GND	GND	GND	SM_GPIO_15	SM_GPIO_14	SM_GPIO_12	GND	GND	CSI4_A0_CLK_M	CSI4_NC_CLK_P	GND	ANT_2G_5G_CH1	D
USB0_CC1	GND	GND	GND	SM_GPIO_13	SM_GPIO_83	GND	GND	GND	GND	GND	GND	GND	GND	C
USB0_SBU2	GND	GND	GND	VREG_L18B_1P8	SM_GPIO_93	GND	GND	GND	GND	GND	GND	GND6		B
USB0_SBU1	GND	GND	GND	VREG_L18B_1P8	GND	GND	ANT_BT_3RD	GND	GND	ANT_2G_5G_CH0	GND			A
15	16	17	18	19	20	21	22	23	24	25	26	27	28	

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2.3 LGA interface pin description

2.3.1 Power supply

Below table describes all interface of SOM power supply and NC pins

Pin name	Pin #	Type	Description
VBATT	A5,A6,A7,A8,B5,B6,B7,B8	PI,PO	Power supply input for SOM. Battery voltage node, output for charging, and input for all operations.
VPH_PWR	C1,C2,C3,D1,D2,D3	PO	Primary system supply node
USB_VBUS	A10,A11,A12,A13,B10,B11,B12,B13	PO,PI	Power entry node for the charger. USB output during USB-OTG operation.
VCOIN	J1,J2	PI,PO	Coin-cell charge and supply recommend to use 22uF for VCOIN
VREG_BOB	AB3,AC3	PO	Buck-boost output 3.3V@1A (will increase to 3.6V during the bootup of the SOM)
VREG_L18B_1P8	A19,B19	PO	PX3, 1.8V Just for GPIO pull-up
VREG_L2C_1P8	W4	PO	MEMS_DMIC_VDD, 1.62V~1.98V, 1.8V type
VREG_L3C_3P0	AA5	PO	Touch screen, 2.7V~3.54V, 3V type
VREG_L4C_1P8_3	V3	PO	Reserved for UIM1, PX5
VREG_L5C_1P8_3	V2	PO	Reserved for UIM2, PX6
VREG_L7C_3P0	AB4	PO	Sensors, 2.7V~3.54V, 3V type
VREG_L8C_1P8	AC4	PO	Sensors, 1.62V~2V, 1.8V type
VREG_L11C_2P8	W3	PO	Connectivity, 1.65V~3.54V, 2.8V type
VREG_L12C_1P8	U2	PO	OLED VDDIO, 1.62V~1.98V, 1.8V type
VREG_L13C_3P0	U3	PO	OLED VCI, 2.7V~3.54V, 2.8V type
VREG_L16B_1P2	H2	PO	1.2V~1.3V, 1.2V typ
VREG_L17B_1P8	N2	PO	WCD_VDD_BUCK, 1.8V~1.9V, 1.8V typ
VREG_SYS_1P8	L1	PO	System 1.8 V I/O output
VIB_DRV_P	F2	PO	Power supply for haptics driver
GND	A3,A4,A9,A14,A16,A17,A18,A20,A21,A23,A24,A26,B3,B4,B9,B14,B16,B17,B18,B21,B22,B23,B24,B25,B26,C14,C16,C17,C18,C21,C22,C23,C24,C25,C26,C27,C28,D9,D13,D14,D16,D17,D18,D19,D23,D24,D27,	GND	GND

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Pin name	Pin #	Type	Description
GND	E27,E28,F12,F18,F27, F28,G9,G10,G16,G17, G18,G21,H3,H9,H16, H17,H18,H19,H21,J9, J16,J18,J21,J25,J26, K9,K26,L9,L20,L26,M1, M9,M19,M21,M22,M25, M26,N9,N10,N20,N21, N22,N25,N26,P1,P2, P9,P10,P19,P20,P21, P22,P25,R10,R11,R17, R18,R19,R20,R21,R22, T9,T17,T18,T19,U9, U17,U18,U19,U25,V9, V12,V13,V14,V15,V16, V17,V18,V19,W1,Y12, Y13,Y22, Y23,Y24,Y25, AA12,AA13,AA14, AA15,AA16,AA17, AA23,AB12,AB19, AC12,AC19,GND1, GND2,GND3,GND4, GND5,GND6,BA1,BA2, BA27,BA28,BB1,BB2,B B27,BB28,BC1,BC2, BC5, BC6, BC7,BC8,BC9,BC10, BC11,BC12,BC13, BC14,BC15,BC16, BC17,BC18,BC19, BC20,BC21,BC22, BC23,BC24,BC25, BC26,BC27,BC28, BD3,BD4,BD5,BD6, BD7,BD8,BD9,BD10, BD11,BD12,BD13, BD14,BD15,BD16, BD17,BD18,BD19, BD25,BD26,BE3,BE5,	GND	GND

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Pin name	Pin #	Type	Description
	BE6,BE7,BE8,BE9, BE10,BE11,BE12, BE13,BE14,BE15, BE16,BE17,BE18, BE19,BE20,BE25, BE26	GND	GND
NC	BC3,BC4,H4,T25,U26, W26	Non	No Connection

2.3.2 Camera interface

SOM supports 5x 4-lane MIPI-CSI interfaces, below table describes pins define

Pin name	Pin #	Volt	Type	Description	Notes
CCI_I2C0_SCL	V21	PX3	DO	Dedicated for camera control I2C (needed PU)	Pull Up at Carrier BD
CCI_I2C0_SDA	V20	PX3	B	Dedicated for camera control I2C (needed PU)	
CAM_MCLK0	M20	CSI	DO	Camera master clock 0	
CSI0_NC_CLK_P	AB26	CSI	AI	MIPI CSI 0 (D-PHY), differential clock – positive	MIPI signals of Camera 0
CSI0_A0_CLK_M	AC26	CSI	AI	MIPI CSI 0 (D-PHY), differential clock – negative	
CSI0_B0_LN0_P	AB25	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 0 – positive	
CSI0_C0_LN0_M	AC25	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 0 – negative	
CSI0_A1_LN1_P	AB24	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – positive	
CSI0_B1_LN1_M	AC24	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – negative	
CSI0_C1_LN2_P	AB23	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – positive	
CSI0_A2_LN2_M	AC23	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – negative	
CSI0_B2_LN3_P	AB22	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 2 – positive	
CSI0_C2_LN3_M	AC22	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 2 – negative	
CCI_I2C1_SCL	V22	PX3	DO	Dedicated for camera control I2C (needed PU)	Pull Up at Carrier BD
CCI_I2C1_SDA	U22	PX3	B	Dedicated for camera control I2C (needed PU)	
CAM_MCLK1	L22	PX3	DO	Camera master clock 1	
CSI1_NC_CLK_P	U28	CSI	AI	MIPI CSI 1 (D-PHY), differential clock – positive	MIPI signals of Camera 1
CSI1_A0_CLK_M	U27	CSI	AI	MIPI CSI 1 (D-PHY), differential clock – negative	
CSI1_B0_LN0_P	V28	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 0 – positive	
CSI1_C0_LN0_M	V27	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 0 – negative	
CSI1_A1_LN1_P	W28	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 1 – positive	
CSI1_B1_LN1_M	W27	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 1 – negative	
CSI1_C1_LN2_P	Y28	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 2 – positive	
CSI1_A2_LN2_M	Y27	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 2 – negative	
CSI1_B2_LN3_P	AA28	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 3– positive	
CSI1_C2_LN3_M	AA27	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 3 – negative	
CCI_I2C2_SCL	T22	PX3	DO	Dedicated for camera control I2C (needed PU)	

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Pin name	Pin #	Volt	Type	Description	Notes
CCI_I2C2_SDA	T21	PX3	B	Dedicated for camera control I2C (needed PU)	Pull Up at
CAM_MCLK2	N19	PX3	DO	Camera master clock 2	
CSI2_NC_CLK_P	M27	CSI	AI	MIPI CSI 2 (D-PHY), differential clock – positive	MIPI signals of Camera 2
CSI2_A0_CLK_M	M28	CSI	AI	MIPI CSI 2 (D-PHY), differential clock – negative	
CSI2_B0_LN0_P	N27	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 0 – positive	
CSI2_C0_LN0_M	N28	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 0 – negative	
CSI2_A1_LN1_P	P27	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 1 – positive	
CSI2_B1_LN1_M	P28	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 1 – negative	
CSI2_C1_LN2_P	R27	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 2 – positive	
CSI2_A2_LN2_M	R28	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 2 – negative	
CSI2_B2_LN3_P	T27	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 3– positive	
CSI2_C2_LN3_M	T28	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 3 – negative	
CCI_I2C3_SCL	U20	PX3	DO	Dedicated for camera control I2C (needed PU)	Pull Up at Carrier BD
CCI_I2C3_SDA	T20	PX3	B	Dedicated for camera control I2C (needed PU)	
CAM_MCLK3	L21	PX3	DO	Camera master clock 3	
CSI3_NC_CLK_P	G27	CSI	AI	MIPI CSI 3 (D-PHY), differential clock – positive	MIPI signals of Camera 3
CSI3_A0_CLK_M	G28	CSI	AI	MIPI CSI 3 (D-PHY), differential clock – negative	
CSI3_B0_LN0_P	H27	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 0 – positive	
CSI3_C0_LN0_M	H28	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 0 – negative	
CSI3_A1_LN1_P	J27	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 1 – positive	
CSI3_B1_LN1_M	J28	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 1 – negative	
CSI3_C1_LN2_P	K27	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 2 – positive	
CSI3_A2_LN2_M	K28	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 2 – negative	
CSI3_B2_LN3_P	L27	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 3– positive	
CSI3_C2_LN3_M	L28	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 3 – negative	
CAM_MCLK4	H20	PX3	DO	Camera master clock 4	
CSI4_A0_CLK_M	D25	CSI	AI	MIPI CSI 4 (D-PHY), differential clock – positive	MIPI signals of Camera 3
CSI4_NC_CLK_P	D26	CSI	AI	MIPI CSI 4 (D-PHY), differential clock – negative	
CSI4_C0_LN0_M	E25	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 0 – positive	
CSI4_B0_LN0_P	E26	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 0 – negative	
CSI4_B1_LN1_M	F25	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 1 – positive	
CSI4_A1_LN1_P	F26	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 1 – negative	
CSI4_A2_LN2_M	G25	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 2 – positive	
CSI4_C1_LN2_P	G26	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 2 – negative	
CSI4_C2_LN3_M	H25	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 3– positive	
CSI4_B2_LN3_P	H26	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 3 – negative	

2.3.3 Display interface

SOM supports 1x 4-lane MIPI-DSI interfaces, below table describes pins define

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Pin name	Pin #	Volt	Type	Description	Notes
DSI0_B1_CLK_P	P8	DSI	AO	MIPI DSI 4 (D-PHY), differential clock – positive	MIPI0 signals for MIPI LCM.
DSI0_C1_CLK_M	P7	DSI	AO	MIPI DSI 4 (D-PHY), differential clock – negative	
DSI0_A0_LN0_P	V8	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 0 – positive	
DSI0_B0_LN0_M	V7	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 0 – negative	
DSI0_C0_LN1_P	R8	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 1 – positive	
DSI0_A1_LN1_M	R7	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 1 – negative	
DSI0_A2_LN2_P	U8	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 2 – positive	
DSI0_B2_LN2_M	U7	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 2 – negative	
DSI0_C2_LN3_P	T8	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 3– positive	
DSI0_NC_LN3_M	T7	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 3 – negative	
EDP0_AUX_P	K7	eDP	B	eDP 1.4 auxiliary channel – positive	DSI and eDP are mutually exclusive
EDP0_AUX_M	K8	eDP	B	eDP 1.4 auxiliary channel – negative	
EDP0_TX0_P	J7	eDP	AO	eDP 1.4 transmit channel 0 – positive	
EDP0_TX0_M	J8	eDP	AO	eDP 1.4 transmit channel 0 – negative	
EDP0_TX1_P	H7	eDP	AO	eDP 1.4 transmit channel 1 – positive	
EDP0_TX1_M	H8	eDP	AO	eDP 1.4 transmit channel 1 – negative	
EDP0_TX2_P	G7	eDP	AO	eDP 1.4 transmit channel 2 – positive	
EDP0_TX2_M	G8	eDP	AO	eDP 1.4 transmit channel 2 – negative	
EDP0_TX3_P	F7	eDP	AO	eDP 1.4 transmit channel 3 – positive	
EDP0_TX3_M	F8	eDP	AO	eDP 1.4 transmit channel 3 – negative	

2.3.4 TouchScreen interface

Touchscreen panels are supported using I2C buses and GPIOs configured as discrete digital inputs

Pin name	Pin #	Volt	Type	Description
SM_GPIO_52	T14	PX3	OD	TP0_SDA
SM_GPIO_53	R15	PX3	OD	TP0_SCL
SM_GPIO_81	N8	PX3	DO	TP0_INT
SM_GPIO_105	J19	PX3	DI	TP0_RST

2.3.5 Audio Interface

The SOM provides sound wire, DMIC and I2S interfaces for audio. Sound wire interface is special for external codec IC, which can build audio functions of the system. DMIC interface can be used to directly connect up to 6 PDM MICs. below table describes pins define

Pin name	Pin #	Volt	Type	Description	Notes
SM_GPIO_144	G14	PX3	DO	Sound wire transmit for WCD	WCD_SWR_TX_CLK
SM_GPIO_145	J13	PX3	DO		WCD_SWR_TX_DATA0

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Pin name	Pin #	Volt	Type	Description	Notes
SM_GPIO_146	G15	PX3	DO		WCD_SWR_TX_DATA1
SM_GPIO_158	F15	PX3	DO		WCD_SWR_TX_DATA3
SM_GPIO_147	F14	PX3	DI	Sound wire receive for WCD	WCD_SWR_RX_CLK
SM_GPIO_148	J12	PX3	DI		WCD_SWR_RX_DATA0
SM_GPIO_149	H13	PX3	DI		WCD_SWR_RX_DATA1
SM_GPIO_154	H11	PX3	IO	AUDIO PA Sound wire	WSA_SWR_CLK
SM_GPIO_155	G12	PX3	IO		WSA_SWR_DATA
SM_GPIO_150	J14	PX3	DO	DMIC I/F	DMIC01_CLK
SM_GPIO_151	H14	PX3	IO		DMIC01_DATA
SM_GPIO_152	J15	PX3	DO		DMIC23_CLK
SM_GPIO_153	H15	PX3	IO		DMIC23_DATA
SM_GPIO_156	F16	PX3	DO		DMIC45_CLK
SM_GPIO_157	F17	PX3	IO		DMIC45_DATA
SM_GPIO_96	R4	PX3	DO	Primary MI²S master clock	PRI_MI2S_MCLK
SM_GPIO_97	P4	PX3	DO	MI2S0	MI2S0_SCK
SM_GPIO_98	N4	PX3	B		MI2S0_DATA0
SM_GPIO_99	M4	PX3	B		MI2S0_DATA1
SM_GPIO_100	R9	PX3	B		MI2S0_WS
SM_GPIO_101	N7	PX3	B	MI2S2	MI2S2_SCK
SM_GPIO_102	R3	PX3	B		MI2S2_DATA0
SM_GPIO_103	L4	PX3	B		MI2S2_WS
SM_GPIO_104	J3	PX3	B		MI2S2_DATA1
SM_GPIO_105	J19	PX3	DO B	MI2S1	SEC_MI2S_MCLK MI2S1_DATA1
SM_GPIO_106	J20	PX3	B		MI2S1_SCK
SM_GPIO_107	K19	PX3	B		MI2S1_DATA0
SM_GPIO_108	K20	PX3	B		MI2S1_WS
SM_GPIO_144	G14	PX3	B	LPI MI2S 4 lanes	LPI_QUA_MI2S_SCK
SM_GPIO_145	J13	PX3	B		LPI_QUA_MI2S_WS
SM_GPIO_146	G15	PX3	B		LPI_QUA_MI2S_DATA0
SM_GPIO_147	F14	PX3	B		LPI_QUA_MI2S_DATA1
SM_GPIO_148	J12	PX3	B		LPI_QUA_MI2S_DATA2
SM_GPIO_149	H13	PX3	B		LPI_QUA_MI2S_DATA3
SM_GPIO_150	J14	PX3	B	LPI I2S1	LPI_I2S1_CLK
SM_GPIO_151	H14	PX3	B		LPI_I2S1_WS
SM_GPIO_152	J15	PX3	B		LPI_I2S1_DATA0
SM_GPIO_153	H15	PX3	B		LPI_I2S1_DATA1
SM_GPIO_154	H11	PX3	B	LPI I2S2	LPI_I2S2_CLK

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Pin name	Pin #	Volt	Type	Description	Notes
SM_GPIO_155	G12	PX3	B		LPI_I2S2_WS
SM_GPIO_156	F16	PX3	B		LPI_I2S2_DATA0
SM_GPIO_157	F17	PX3	B		LPI_I2S2_DATA1

2.3.6 USB & DisplayPort interface

The SOM supports 1x USB 3.1 GEN1, with Type-C with DisplayPort and 1x USB2.0.

Pin name	Pin #	Type	Description	Notes
PM_USB_OPTION	G2	AI	Used to select different PON options based on pull-down (PD) resistor value Configuration selection for micro-USB and Type-C connectors. Float for Type-C and connect to ground with 0 Ohm for micro USB.	
USB_THERM	E1	AI	USB Type-C connector temperature sensor	
USB_SS-H_HS-L_SEL	AA11	DI	Connected to ID Pin of Micro USB. Not supported on SOM by default.	
USB0_CC1	C15	AI, PO	CC1 Pin for the USB Type-C connector or OTG mode enable	
USB0_CC2	D15	AI, PO	CC2 Pin for the USB Type-C connector	
USB0_SBU1	A15	DI	Type-C side band signal SBU1; protected to 22 V max.	
USB0_SBU2	B15	DO	Type-C side band signal SBU2; protected to 22 V max.	
USB0_DP_AUX_P	AB17	AI, AO	DisplayPort auxiliary channel – positive	Native DP
USB0_DP_AUX_M	AC17	AI, AO	DisplayPort auxiliary channel – negative	
USB0_HS_DP	F1	AI, AO	USB 2.0 high-speed data – positive	
USB0_HS_DM	G1	AI, AO	USB 2.0 high-speed data – negative	
USB0_SS_TX0_P	AB14	AO	USB 3.0 Type C PHY transmit 0 – positive	
USB0_SS_TX0_M	AC14	AO	USB 3.0 Type C PHY transmit 0 – negative	
USB0_SS_RX0_P	AB13	AI	USB 3.0 Type C PHY receiver 0 – positive	
USB0_SS_RX0_M	AC13	AI	USB 3.0 Type C PHY receiver 0 – negative	
USB0_SS_TX1_P	AB15	AO	USB 3.0 Type C PHY transmit 1 – positive	
USB0_SS_TX1_M	AC15	AO	USB 3.0 Type C PHY transmit 1 – negative	
USB0_SS_RX1_P	AC16	AI	USB 3.0 Type C PHY receiver 1 – positive	
USB0_SS_RX1_M	AB16	AI	USB 3.0 Type C PHY receiver 1 – negative	

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USB1_HS_DP	AC18	AI, AO	USB1_HS – positive	USB1 2.0
USB1_HS_DM	AB18	AI, AO	USB1_HS – negative	

2.3.7 PCIe interface

The SOM supports one Peripheral Component Interconnect Express (PCIe) interfaces, which can be used for general-purpose peripherals.

Pin name	Pin #	Voltage	Type	Description
PCIE1_REFCLK_P	AC11	PCIe	AI,AO	PCIe 1 Gen 3 reference clock – positive
PCIE1_REFCLK_M	AB11	PCIe	AI,AO	PCIe 1 Gen 3 receive lane 0 – negative
PCIE1_TX0_P	AC7	PCIe	AO	PCIe 1 Gen 3 Transmit lane 0– positive
PCIE1_TX0_M	AB7	PCIe	AO	PCIe 1 Gen 3 Transmit lane 0– negative
PCIE1_RX0_P	AC8	PCIe	AI	PCIe 1 Gen 3 receive lane 0 – positive
PCIE1_RX0_M	AB8	PCIe	AI	PCIe 1 Gen 3 receive lane 0 – negative
PCIE1_TX1_P	AC9	PCIe	AO	PCIe 1 Gen 3 Transmit lane 1– positive
PCIE1_TX1_M	AB9	PCIe	AO	PCIe 1 Gen 3 Transmit lane 1– negative
PCIE1_RX1_P	AC10	PCIe	AI	PCIe 1 Gen 3 receive lane 1 – positive
PCIE1_RX1_M	AB10	PCIe	AI	PCIe 1 Gen 3 receive lane 1 – negative
PCIE1_CLK_REQ_N	Y16	PX3	DI	PCIe Clock request
PCIE1_RESET_N	Y14	PX3	DO	PCIe reset signal
PCIE1_WAKE_N	Y15	PX3	DI	PCIe wake up signal
PCIE0_TX_P	BE23	PCIe	AO	PCIe 0 Gen 3 Transmit lane– positive
PCIE0_TX_M	BD23	PCIe	AO	PCIe 0 Gen 3 Transmit lane– negative
PCIE0_RX_P	BE24	PCIe	AI	PCIe 0 Gen 3 receive lane– positive
PCIE0_RX_M	BD24	PCIe	AI	PCIe 0 Gen 3 receive lane– negative
PCIE0_RESET_N	BE21	PX3	DO	PCIe reset signal
PCIE0_WAKE_N	BD21	PX3	DI	PCIe wake up signal
PCIE0_REFCLK_P	BE22	PCIe	AI,AO	PCIe 0 Gen 3 reference clock – positive
PCIE0_REFCLK_M	BD22	PCIe	AI,AO	PCIe 0 Gen 3 receive lane 0 – negative
PCIE0_CLK_REQ_N	BD20	PX3	DI	PCIe Clock request

2.3.8 SDIO interface

The SOM supports 1 x 4-lane SDIO, SDC2 connected to SD card.

The SDIO is a high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on)

- The clock can be up to 200 MHz
- The signals routing should be 50Ω ±10% impedance control.

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- CLK to DATA/CMD length matching less than 1mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

Pin name	Pin #	Volt.	Type	Description	Notes
VREG_L9C_2P96	Y5	-	PO	SD Card Power Supply	
VREG_L6C_2P96	Y4	-	PO	SD Card pull up power	
SDC2_CLK	T10	PX2	DO	SD controller 2 clock	
SDC2_CMD	T11	PX2	DO-NP:pdpukp	SD controller 2 command	
SDC2_DATA_0	V11	PX2	BH-NP:pdpukp	SD controller 2 data bit 0	
SDC2_DATA_1	U10	PX2	BH-NP:pdpukp	SD controller 2 data bit 1	
SDC2_DATA_2	V10	PX2	BH-NP:pdpukp	SD controller 2 data bit 2	
SDC2_DATA_3	U11	PX2	BH-NP:pdpukp	SD controller 2 data bit 3	
SD_CARD_DET_N	M10	PX3	BH-NP:pdpukp	Insert detection	SM_GPIO_91

2.3.9 SSC interface

The SOM has an integrated sensor subsystem called Snapdragon™ sensor core (SSC), which is dedicated to support low-power, always-on use cases.

The sensor subsystem can be left powered on even when the rest of the MSM device is in sleep mode.

The SSC core has dedicated I/O to communicate with the sensors. The I/O scan support I2C and SPI interfaces.

Pin name	Pin #	Volt.	Type	Description	Notes
SNS_I3C0_SDA	K10	PX3	BIO	These I3C signals are dedicated to Sensor	SM_GPIO_159
SNS_I3C0_SCL	L10	PX3	BIO		SM_GPIO_160
SNS1_I2C_SDA	H10	PX3	BIO	These I2C signals are dedicated to Sensor	SM_GPIO_161
SNS1_I2C_SCL	J10	PX3	BIO		SM_GPIO_162
SM_GPIO_163	J11	PX3	BIO	Snapdragon™ Sensor Core SPI signals	SM_GPIO_163
SM_GPIO_164	H12	PX3	BIO		SM_GPIO_164
SM_GPIO_165	F13	PX3	BIO		SM_GPIO_165
SM_GPIO_166	G13	PX3	BIO		SM_GPIO_166

2.3.10 QUP interface

These GPIOs are available as QUP (Qualcomm universal peripheral) interface ports that can be configured for UART, SPI, I2C or I3C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus needs to be supplemented by a 2.2 KΩ pull-up resistor.

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Pin name	Pin #	Volt.	Type	Description	Notes
SM_GPIO_0	G19	PX3	BIO	QUP0 SE0 Lane0/1	
SM_GPIO_1	G20	PX3	BIO		
PCIE1_RESET_N	Y14	PX3	BIO	QUP0 SE0 Lane2/3	SM_GPIO_2
PCIE1_WAKE_N	Y15	PX3	BIO	QUP0 SE7 Lane4/5	SM_GPIO_3
APPS_I2C_SDA	Y18	PX3	BIO	QUP0 SE1 Lane0/1	SM_GPIO_4
APPS_I2C_SCL	Y17	PX3	BIO		SM_GPIO_5
SM_GPIO_6	K21	PX3	BIO	QUP0 SE0 Lane2 QUP0 SE7 Lane6	
SM_GPIO_7	K25	PX3	BIO	QUP0 SE1 Lane3	
SM_GPIO_8	L25	PX3	BIO	QUP0 SE2 Lane0/1	
SM_GPIO_9	R25	PX3	BIO		
SM_GPIO_12	D22	PX3	BIO	QUP0 SE3	
SM_GPIO_13	C19	PX3	BIO		
SM_GPIO_14	D21	PX3	BIO		
SM_GPIO_15	D20	PX3	BIO		
SM_GPIO_16	H22	PX3	BIO	QUP0 SE4	
SM_GPIO_17	J22	PX3	BIO		
SM_GPIO_18	F22	PX3	BIO		
SM_GPIO_19	G22	PX3	BIO		
SM_GPIO_20	AA24	PX3	BIO	QUP0 SE5	
SM_GPIO_21	AB21	PX3	BIO		
DBG_UART_TX	AB20	PX3	BIO		SM_GPIO_22
DBG_UART_RX	AC20	PX3	BIO		SM_GPIO_23
SM_GPIO_24	V26	PX3	BIO	QUP0 SE6	
SM_GPIO_25	Y26	PX3	BIO		
SM_GPIO_32	L19	PX3	BIO	QUP1 SE0	
SM_GPIO_33	R12	PX3	BIO		
SM_GPIO_34	T12	PX3	BIO		
SM_GPIO_35	R13	PX3	BIO		
SM_GPIO_36	T15	PX3	BIO	QUP1 SE1	
SM_GPIO_37	T16	PX3	BIO		
SM_GPIO_38	U15	PX3	BIO		
SM_GPIO_39	U16	PX3	BIO		
SM_GPIO_40	M3	PX3	BIO	QUP1 SE2	
SM_GPIO_41	N3	PX3	BIO		
SM_GPIO_42	K2	PX3	BIO		
SM_GPIO_43	H1	PX3	BIO		
SM_GPIO_44	T13	PX3	BIO	QUP1 SE3	

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Pin name	Pin #	Volt.	Type	Description	Notes
SM_GPIO_45	U12	PX3	BIO		
SM_GPIO_46	R14	PX3	BIO		
SM_GPIO_47	U13	PX3	BIO		
SM_GPIO_48	P3	PX3	BIO	QUP1 SE4	
SM_GPIO_49	K1	PX3	BIO		
SM_GPIO_50	L2	PX3	BIO		
SM_GPIO_51	M2	PX3	BIO		
SM_GPIO_52	T14	PX3	BIO	QUP1 SE5	
SM_GPIO_53	R15	PX3	BIO		
SM_GPIO_54	U14	PX3	BIO		
SM_GPIO_55	R16	PX3	BIO		
SM_GPIO_56	R1	PX3	BIO	QUP1 SE6	
SM_GPIO_57	R2	PX3	BIO		
SM_GPIO_58	T2	PX3	BIO		
SM_GPIO_59	T1	PX3	BIO		
SM_GPIO_60	AC6	PX3	BIO	QUP1 SE7 Lane0/1	
SM_GPIO_61	AB5	PX3	BIO		
SM_GPIO_62	AA6	PX3	BIO	QUP1 SE7 Lane2/SE6 Lane4	
SM_GPIO_63	AC5	PX3	BIO	QUP1 SE6 Lane3/SE6 Lane5	

2.3.11 Debug UART interface

Pin name	Pin #	Volt.	Type	Description	Notes
DBG_UART_TX	AB20	PX3	DO	QUP0 SE5 UART signals, can use for debug	SM_GPIO_22
DBG_UART_RX	AC20	PX3	DI		SM_GPIO_23

2.3.12 Power on interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the available power sources of the device, and enable the correct source. Press the KPD_PWR_N for ~2 s to boot the system properly. Power on/off key signal can be connected to ground through SOM Pin M8, PHONE_ON_N (200 KΩ internally pulled up to 1.1 V).

Pin name	Pin #	Volt.	Type	Description	Notes
PHONE_ON_N	M8	-	DI	Power-on key ground switch (200 KΩ internal PU to 1.1 V)	

2.3.13 Reset interface

You can generate a mandatory reset by a long key press of RESIN_N,

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KPD_PWR_N, or RESIN_N plus KPD_PWR_N in combination.

Pin name	Pin #	Volt.	Type	Description	Notes
PM_RESIN_N	L8	-	DI	Volume down/Reset key signal, Low active (40 KΩ internal PU to 1.8 V)	

2.3.14 Keys interface

Pin name	Pin #	Volt.	Type	Description	Notes
PM_RESIN_N	L8	-	DI	Volume down/Reset key signal, Low active (40 KΩ internal PU to 1.8 V)	
PHONE_ON_N	M8	-	DI	Power-on key ground switch (200 KΩ internal PU to 1.1 V)	
KYPD_VOL_UP_N	L7	-	DI	Keypad volume up button	

2.3.15 Battery interface

Battery interfaces are special for battery interface, major for monitoring battery status, inserting and voltage detection

Pin name	Pin #	Volt.	Type	Description	Notes
BATT_THERM	C6	1.875V max	AI	Battery temperature input to ADC for measuring the pack temperature. Used for charger safe operation and BMS. 100K pull down, or connect to Battery	
BATT_ID	C4	1.875V max	AI	Battery ID input to the ADC interface. Used for missing battery detection. 100K pull down, or connect to Battery	
VBATT_VSNS_P	E3	-	AI	Battery voltage sense input plus. Connect to the battery positive remote sense node or connect this directly to the battery positive node.	
VBATT_VSNS_M	F3	-	AI	Battery voltage sense input minus. Connect to the battery negative remote sense node or connect this directly to the battery negative node.	
VBATT_PACK_SNS_M	C5	-	AI	Battery voltage sense input minus. Directly to the battery negative node (pack negative).	
VBATT_OPT_ISNS_P	D4	-	AI	Reserved	
VBATT_OPT_ISNS_M	D6	-	AI	Reserved	

2.3.16 GPIO

These GPIOs are configurable as Input or Output with pull-up (PU), pull-down (PD), open-drain (NP), or keeper (KP) cell structure. The setting of default and option IO structure are listed for each GPIO in below table..

Pin name	Pin #	Volt.	Type	Description	Notes
SM_GPIO_51	M2	PX3	BIO	PD:nppukp (Default:option)	QUP1 SE4, lane 3

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Pin name	Pin #	Volt.	Type	Description	Notes
SM_GPIO_54	U14	PX3	BIO	PD:nppukp	QUP1 SE4, lane 5
SM_GPIO_55	R16	PX3	BIO	PD:nppukp	QUP1 SE4, lane 4
SM_GPIO_56	R1	PX3	BIO	PD:nppukp	QUP1 SE6, lane 0
SM_GPIO_57	R2	PX3	BIO	PD:nppukp	QUP1 SE6, lane 1
SM_GPIO_58	T2	PX3	BIO	PD:nppukp	QUP1 SE6, lane 2
SM_GPIO_59	T1	PX3	BIO	PU:nppdkp	QUP1 SE6, lane 3
SM_GPIO_60	AC6	PX3	BIO	PD:nppukp	QUP1 SE7, lane 0
SM_GPIO_61	AB5	PX3	BIO	PD:nppukp	QUP1 SE7, lane 1
SM_GPIO_62	AA6	PX3	BIO	PD:nppukp	QUP1 SE7, lane 2
SM_GPIO_63	AC5	PX3	BIO	PD:nppukp	QUP1 SE7, lane 3
SM_GPIO_77	U21	PX3	BIO	PD:nppukp	
SM_GPIO_78	R26	PX3	BIO	PD:nppukp	
SM_GPIO_80	N1	PX3	BIO	PD:nppukp	
SM_GPIO_83	C20	PX3	BIO	PD:nppukp	BOOT_CONFIG[8]
SM_GPIO_90	P26	PX3	BIO	PD:nppukp	
SM_GPIO_93	B20	PX3	BIO	PD:nppukp	BOOT_CONFIG[13]
SM_GPIO_109	Y7	PX6	BIO	PD:nppukp	UIM2_DATA
SM_GPIO_110	Y8	PX6	BIO	PD:nppukp	UIM2_CLK
SM_GPIO_111	AA7	PX6	BIO	PD:nppukp	UIM2_RESET
SM_GPIO_112	AA8	PX3	BIO	PD:nppukp	UIM2_PRESENT
SM_GPIO_113	Y9	PX5	BIO	PD:nppukp	UIM1_DATA
SM_GPIO_114	Y10	PX5	BIO	PD:nppukp	UIM1_CLK
SM_GPIO_115	AA9	PX5	BIO	PD:nppukp	UIM1_RESET
SM_GPIO_116	AA10	PX3	BIO	PD:nppukp	UIM1_PRESENT
SM_GPIO_117	Y21	PX3	BIO	PD:nppukp	
SM_GPIO_118	AA21	PX3	BIO	PD:nppukp	BOOT_CONFIG[0]
SM_GPIO_119	Y20	PX3	BIO	PD:nppukp	
SM_GPIO_120	AA20	PX3	BIO	PD:nppukp	BOOT_CONFIG[1]
SM_GPIO_122	T26	PX3	BIO	PD:nppukp	BOOT_CONFIG[2]
SM_GPIO_123	Y19	PX3	BIO	PD:nppukp	
SM_GPIO_124	AA19	PX3	BIO	PD:nppukp	BOOT_CONFIG[3]
SM_GPIO_129	AA18	PX3	BIO	PD:nppukp	
SM_GPIO_130	AA25	PX3	BIO	PD:nppukp	BOOT_CONFIG[7]
SM_GPIO_131	AA22	PX3	BIO	PD:nppukp	BOOT_CONFIG[5]
SM_GPIO_132	K22	PX3	BIO	PD:nppukp	BOOT_CONFIG[6]
SM_GPIO_136	F19	PX3	BIO	PD:nppukp	
SM_GPIO_137	F20	PX3	BIO	PD:nppukp	
SM_GPIO_138	F21	PX3	BIO	PD:nppukp	BOOT_CONFIG[15]

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Pin name	Pin #	Volt.	Type	Description	Notes
SM_GPIO_141	AB6	PX3	BIO	PD:nppukp	
SM_GPIO_142	Y11	PX3	BIO	PD:nppukp	

2.3.17 PMIC GPIO

The PMICs provide GPIO with different functions. below table describes pins define of each PMIC GPIO

PMK7325

Pin name	Pin #	Volt.	Type	Description	Notes
PMK_GPIO_01	V25	LV	B	Configurable; default digital input with 10µA pull-down	AMUX SMB_SPMI_CLK
PMK_GPIO_02	W25	LV	B	Configurable; default digital input with 10µA pull-down	AMUX SMB_SPMI_DATA

PM7250B

Pin name	Pin #	Volt.	Type	Description	Notes
PM_A_GPIO_01	F10	LV	B	Configurable; default digital input with 10µA pull-down Interrupt	PM7250B_GPIO_1
PM_A_GPIO_02	G4	LV	B	Configurable; default digital input with 10µA pull-down	PM7250B_GPIO_2
PM_A_GPIO_03	F9	LV	B	Configurable; default digital input with 10µA pull-down	PM7250B_GPIO_3
PM_A_GPIO_04	G3	LV	B	Configurable; default digital input with 10µA pull-down	PM7250B_GPIO_4
PM_A_GPIO_05	C9	MV	B	Configurable; default digital input with 10µA pull-down	PM7250B_GPIO_5
PM_A_GPIO_06	D5	MV	B	Configurable; default digital input with 10µA pull-down	PM7250B_GPIO_6
PM_A_GPIO_07	F4	MV	B	Configurable; default digital input with 10µA pull-down	PM7250B_GPIO_7
PM_A_GPIO_08	E2	MV	B	Configurable; default digital input with 10µA pull-down	PM7250B_GPIO_8
PM_A_GPIO_09	D8	LV	B	Configurable; default digital output, open drain	PM7250B_GPIO_9
PM_A_GPIO_10	G11	LV	B	Configurable; default digital output, open drain	PM7250B_GPIO_10

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Pin name	Pin #	Volt.	Type	Description	Notes
PM_A_GPIO_11	E4	LV	B	Configurable; default digital input with 10µA pull-down	PM7250B_GPIO_11
PM_A_GPIO_12	F11	LV	B	Configurable; default digital input with 10µA pull-down	PM7250B_GPIO_12

PM7325

Pin name	Pin #	Volt.	Type	Description	Notes
PM_B_GPIO_08	J4	MV	B	Configurable; default digital input with 10µA pull-down	PM7325_GPIO_08
PM_B_GPIO_09	K4	MV	B	Configurable; default digital input with 10µA pull-down	PM7325_GPIO_09
PM_B_AMUX2	K3		AI	Analog multiplexer (AMUX) input 2	AMUX_2
PM_B_AMUX4	L3		AI	Analog multiplexer (AMUX) input 4	AMUX_4

PM7350C

Pin name	Pin #	Volt.	Type	Description	Notes
PM_C_GPIO_01	W2	LV	B	Configurable; default digital input with 10µA pull-down	
PM_C_GPIO_02	V4	LV	B	Configurable; default digital input with 10µA pull-down	
PM_C_GPIO_03	W5	LV	B	Configurable; default digital input with 10µA pull-down	
PM_C_GPIO_04	Y6	LV	B	Configurable; default digital input with 10µA pull-down	
PM_C_GPIO_05	T3	MV	B	Configurable; default digital input with 10µA pull-down	
PM_C_GPIO_06	V1	MV	B	Configurable; default digital input with 10µA pull-down	
PM_C_GPIO_07	U1	MV	B	Configurable; default digital input with 10µA pull-down	
PM_C_GPIO_08	U4	MV	B	Configurable; default digital input with 10µA pull-down	
PM_C_GPIO_09	T4	MV	B	Configurable; default digital input with 10µA pull-down	

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2.3.18 PMB and SMB option reservation

Some LGA pins are listed in below table, those are used for external Charger, SMB , PMIC of Qualcomm solutions as reservation.

Pin name	Pin #	Description	Pin name	Pin #	Description
PMB_MID_CHG_1	C10		PMB_DC_IN_PON	D10	
PMB_MID_CHG_2	C11		PMB_DC_IN_PSNS	D11	
PMB_MID_CHG_3	C12		PMB_DC_IN_EN	D12	
PMB_MID_CHG_4	C13		SMB_THERM	C7	
FAULT_N	AC21		SMB_ICHG_FB	C8	
			SMB_EN	D7	

2.3.19 PWMs and LED current driver interface

The SOM has two PWM outputs and three LED Current Drivers

Pin name	Pin #	Volt.	Type	Description	Notes
PWM signals					
PM_C_GPIO_08	U4	MV	DO	Can be configured as GPIO and PWM (only GPIO_08 is available for fixed duty cycle variable frequency mode)	
PM_C_GPIO_09	T4	MV	DO		
LED signals					
IRIS_RED	AA3	-	AO	Independent high-side current source brightness control of Red, Green, and Blue channels, 12 mA maximum per channel	
IRIS_GREEN	AA4	-	AO		
IRIS_BLUE	Y3	-	AO		
FLASH LED signals					
FLASH_LED1	AA1,AA2	-	AO	Flash high-side current source	
FLASH_LED2	Y1,Y2	-	AO		

2.3.20 RF interface (N.A)

The SOM provides the fully-integrated WLAN and Bluetooth function those are not available in this version.

Antenna Interface

Pin Name	Pin #	Description	Notes
ANT_2G_5G_CH0	A25	Antenna 1 supports WLAN/BT RF 2.4GHz/5GHz/6GHz Chain 0	Chain 0
ANT_2G_5G_CH1	D28	Antenna 2 supports WLAN/BT RF 2.4GHz/5GHz/6GHz Chain 1	Chain 1
RF_ANT_GNSS	BE4	Antenna supports GNSS L1/L5	-

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WCN interface

Pin Name	Pin #	Description	Notes
WCN_SDR_N79 _TO_TXEN	J24	This pin is an input from the SDR to the WCN6750. This GPIO is set high by the SDR when N79 transmits above a prescribed RF power. The WCN6750 can be configured to respond to this GPIO when operating below a certain channel number, and to ignore this GPIO when operating above a certain channel number. When the WCN6750 responds to this GPIO, it places the 5 GHz receivers in a protected state to prevent damage.	
WCN_SDR_TXEN _TO_N79	K24	This is an output from the WCN6750 to the SDR. The WCN6750 asserts this GPIO to high state when the 5 GHz or 6 GHz chains are transmitting about certain power, and below a configurable channel frequency. The intent of allowing the channel to be configured is to improve concurrency with N79, depending on the filter selected and used on the device.	
WCN_SDR_LAA _TO_TXEN	L24	This is an input from the SDR to the WCN6750. The SDR sets GPIO high if LAA is transmitting. GPIO is monitored by WCN6750. When it goes high, WCN6750 places the 5 GHz receiver in a protected state. SRD sets high when LAA transmits at 10 dBm or higher. This pin is monitored even in sleep mode, as long as the 0.8 V AON domain is powered.	
WCN_SDR_TXEN_ TO_LAA	M24	This is an output from the WCN6750 to the SDR. The WCN6750 asserts this GPIO to high state, when either 5 GHz chain 0 or chain 1 is set to transmit at power greater than 10 dBm. When this GPIO is set high, the LAA receivers are placed in a protected state.	

2.3.21 Miscellaneous

This section has listed some signals on LGA for function reservation, but not be grouped in others signals.

Pin name	Pin #	Volt.	Type	Description	Notes
LNBBCLK2	AA26	PX3	DO	Clock for external NFC option	
SLEEP_CLK	J17	PX3	DI	Used for WCN in sleep mode	
FORCED_USB_BOOT	M7	PX3	DI	Force H at power on period to enter USB Boot	POLARITY_SEL=L in SOM

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

The absolute maximum ratings in which the SOM input power sources can be exposed to without experiencing functional failure.

Function	Min	Max	Unit
SOM input voltage	-0.3	6	V
USB VBUS	-0.3	28	V

3.2 Operating conditions

The recommended operating conditions for the SOM to meet all performance specifications (provided the absolute maximum ratings have never been exceeded)

Function	Min	Typ.	Max	Unit
SOM input voltage	2.7	3.8	4.8	V
USB VBUS	3.7	5	12.6	V

3.3 Output Voltages

The SOM provide voltage supply for external device, like camera module, SD card, Sensor, and so on. Below map show the details

Function	Pin #	Volt(V)	Range (V)	Usage
VPH_PWR	C1,C2,C3 D1,D2,D3	-	+3.2~4.75	Primary system supply node
VREG_BOB	AB3,AC3	+3.3	-	Buck-boost output 3.3V@1A
VREG_L18B_1P8	A19,B19	+1.8	+1.8~2.0	PX3, 1.8V for GPIO Pull-up
VREG_L2C_1P8	W4	+1.8	+1.62~1.98	MEMS_DMIC_VDD, 1.8V typ
VREG_L3C_3P0	AA5	+3.008	+2.8~3.54	Touch screen, 3V typ
VREG_L7C_3P0	AB4	+3.008	+2.8~3.54	Sensors, 3V typ
VREG_L8C_1P8	AC4	+1.8	+1.8~2.0	Sensors, 1.8V typ
VREG_L11C_2P8	W3	+2.8	+2.8~3.54	Connectivity, 2.8V typ
VREG_L12C_1P8	U2	+1.8	+1.8~1.98	OLED VDDIO, 1.8V typ
VREG_L13C_3P0	U3	+3.0	+2.7~3.54	OLED VCI, 2.8v typ
VREG_L16B_1P2	H2	+1.2	+1.2~1.3	1.2V typ
VREG_L17B_1P8	N2	+1.8	+1.8~1.9	WCD_VDD_BUCK, 1.8V typ
VREG_SYS_1P8	L1	-	+1.75~1.86	System 1.8V I/O output
VIB_DRV_P	F2	TBD	TBD	Power supply for haptics driver

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3.4 GPIO characteristics

The below table shows the GPIO characteristics (VDDPX3=1.8V)

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	VDDPX3 x0.65	VDDPX3 +0.3	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3	VDDPX3 x0.35	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	VDDPX3 x0.7	VDDPX3 +0.3	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3	VDDPX3 x0.3	V
V_{HYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	-	mV
V_{HYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	-	mV
V_{OH}	High-level output voltage, CMOS	VDDPX3 -0.45	VDDPX3	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V
I_{ILPU}	Input low leakage current with Pull-up	-97.5 (20)	-27.5 (60)	uA (KΩ)
I_{IHPD}	Input high leakage current with Pull-down	27.5 (60)	97.5 (20)	uA (KΩ)

The below table shows the SD card IO characteristics (VDDPX2=1.8V / 2.96V)

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage, CMOS/Schmitt	1.27/ VDDPX2 x0.625	2,0/ VDDPX2 +0.3	V
V_{IL}	Low-level input voltage, CMOS/Schmitt	-0.3/ -0.3	0.58/ VDDPX2 x0.25	V
V_{SHYS}	Schmitt hysteresis voltage	100	-	mV
V_{OH}	High-level output voltage	1.4/ VDDPX2 x0.75	-/ VDDPX2	V
V_{OL}	Low-level output voltage	0/ 0	0.45/ VDDPX2 x0.125	V
$R_{PULL-UP}$	Pull-up resistance	10	100	KΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	100	KΩ

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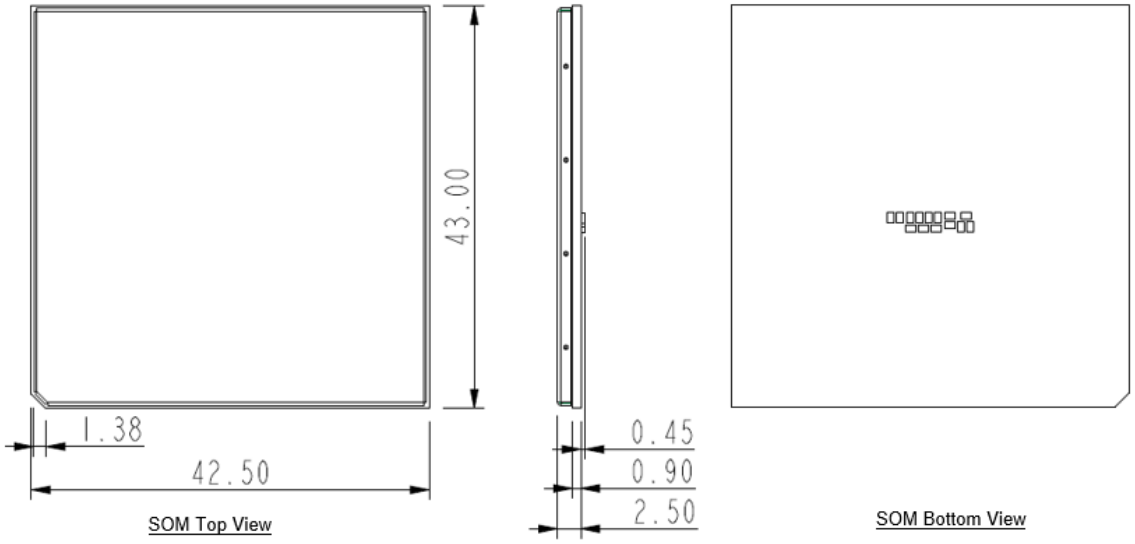
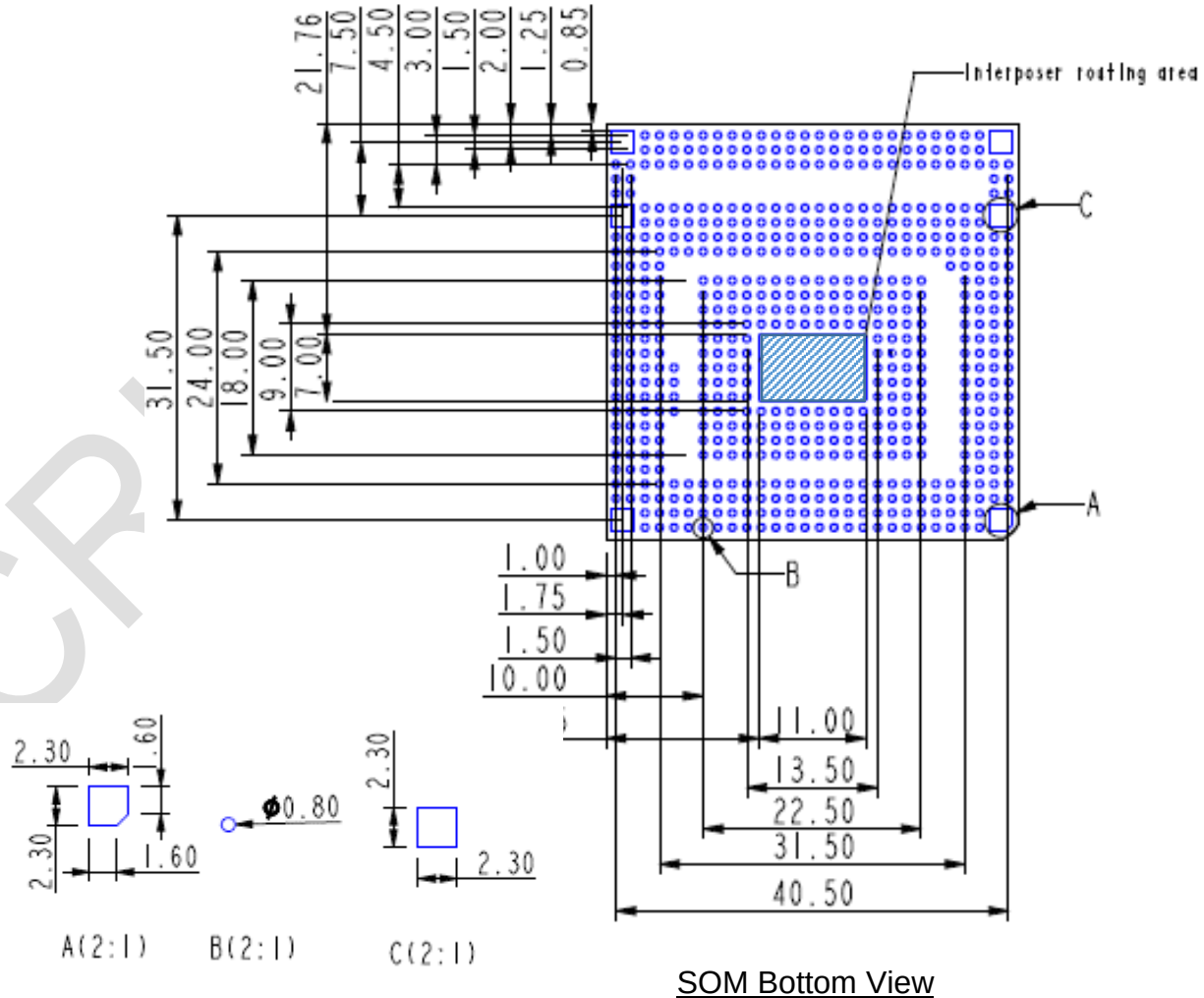
4. Mechanical Specification

4.1 SOM Mechanical dimensions



SOM Top View

SOM Bottom View



SOM Bottom View

4.2 Weight

The SOM weighs approximately 12 +/- 2 g

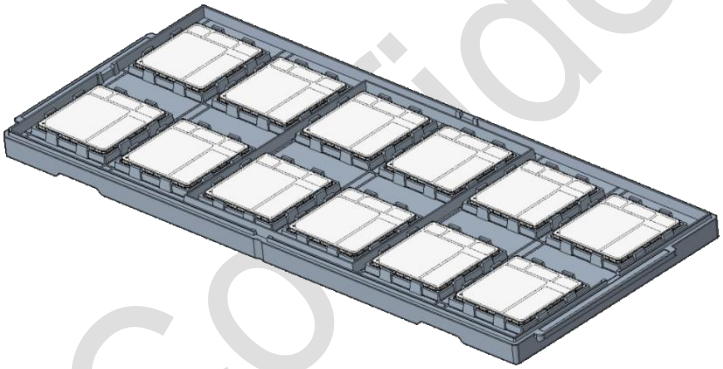
4.3 Thermal Characteristics

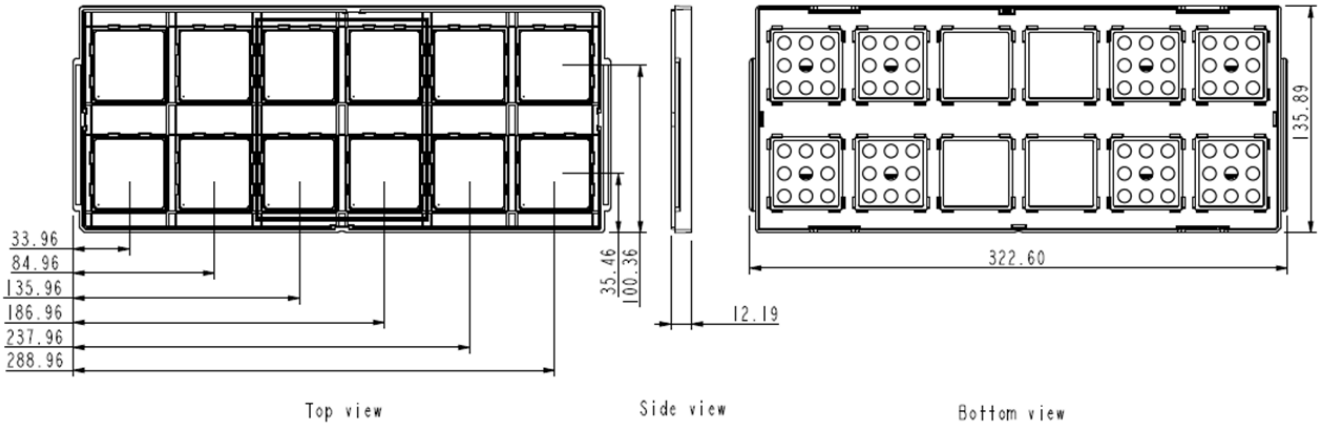
Please refer “Thermal Testing and Result” of Qualcomm public document as reference through below URL

https://docs.qualcomm.com/bundle/publicresource/topics/80-70015-251/thermal_testing.html

4.4 Packaging Information

The Packaging of LGA SOM is shown in below picture, each tray can be placed 12 pcs SOM, then stacked as 11 layers including top layer as cover tray, and then put into vacuum bag. Each bag is packed with 120 pcs (12 x 10) LGA SOM, and then EPE is used as cushioning material for shock protection as a formal unit packaging.





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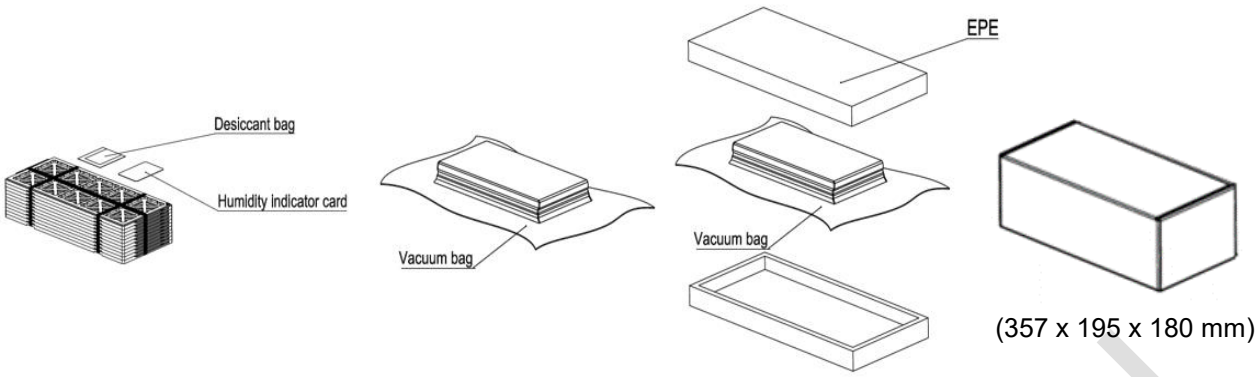
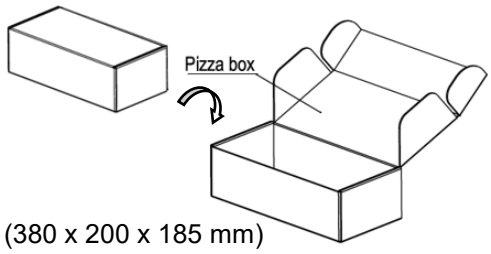
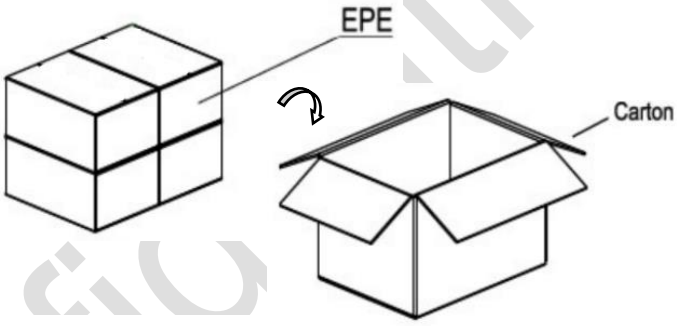


Two kinds shipping package has be provided, one is packed with one formal unit for 120 (or less) pcs based, another one is packed with 4 formal unit for 480 pcs based.

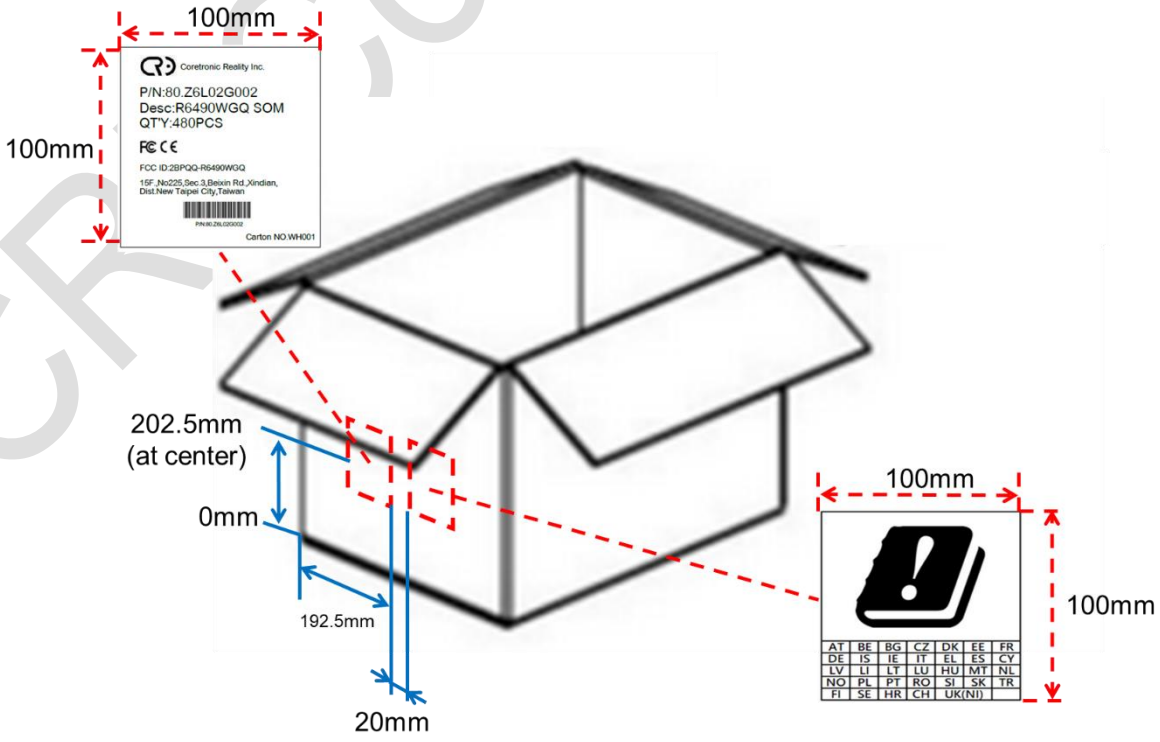


Shipping package for 120 pcs (or less) based



Shipping package for 480 pcs (or less) based

Outbox Carton Label :



4.5 Temperature and Humidity

Operation Temperature: -20°C to +70°C
(Max Tj must be kept below 95°C to prevent SoC throttling)
Operation Humidity: < 90% RH
Storage Temperature: -40°C to +80°C
Storage Humidity: < 90% RH

5. Product Marking

Model Number : R6490Q / R5430Q

Serial Number : (by QR code with D/C + S/N)

Part Number : SP.Z6L22G00x (R6490Q)
/ SP.Z6L24G00x (R5430Q)
x means revision number of SOM

6. Compliance Statements

MSL (Moisture Sensitivity Level) :
The moisture sensitivity level of this product is rated at MSL Level 2a.

Strategic Hi-Tech Commodity (SHTC) :
☐ Yes (Y) / ■ No (N) , This product is not intended for use in military application.

RoHS Statement :
This product complies with the EU RoHS Directive (2011/65/EU and its amendments) and does not contain restricted hazardous substances.

Halogen-free Statement :
This product meets halogen-free requirements and does not contain halogen elements such as chlorine (Cl) or bromine (Br).

REACH 247 Statement :
This product does not contain any of the 247 substances of very high concern (SVHCs) listed under the EU REACH regulation.

CMRT v6.5 :
The company adheres to the Conflict Minerals Reporting Template (CMRT v6.5) developed by the Responsible Minerals Initiative (RMI) to disclose the sources of tin (Sn), tantalum (Ta), tungsten (W), and gold (Au). Does this product contain conflict minerals: ☐ Yes / ■ No

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